

3033 Processor Complex

Description

The IBM System/370 3033 Processor Complex is a large scale system with virtual storage capabilities. It consists of a system console, a power and cooling element, plus five other logical elements:

- Instruction Preprocessing Function

 fetches instructions from processor

 storage and prepares them for execution.
- E-function executes the arithmetic, logical and some control and decision functions of the System/370 instructions.
- Processor Strorage Control Function and Processor Storage processes all requests to store data or fetch data from processor storage, for a channel or for instruction processing.
- Channels the basic system contains 12 channels (expandable to 16) with integrated channel controls and fixed addresses.
- Maintenance Controls detection of certain types of machine errors results in a retry of the processing function and a logout of the condition encountered.

Compatibility

The 3033 is upward program compatible with current System/360 and System/370 without extensive reprogramming with the following exceptions:

- Programs using model-dependent data.
- Programs using model-dependent features or devices not available on this system.
- Programs that depend on validity of data after system power has been turned off and restored.
- □ System/360 programs using ASCII bit (PSW bit 12)
- Programs which contain time dependencies.

Maintainability

Maintenance of the 3033 Processor Complex is dependent on the following facilities:

- □ Extensive error checking and indicators.
- A Support Console to display significant control and status latches/triggers. Also provides capability to dynamically retrieve and manipulate log and trace data.
- ☐ The last 12 processor machine check logs the last 12 logs per channel group, the last 12 trace/events and 1K bytes of power messages are recorded for retrieval by the on-site CE or Remote Specialist.
- Logout analysis program for resolution of intermittent failures.
- Processor microdiagnostics and other conventional software diagnostics for fault location,
- De Power controlled by the Support Facility.
- □ Marginal checking of processor logic.
- A divice using a magnetic disk cartridge to load microdiagnostics via a dedicated path.
- Retain/370 with data bank and remote technical assist capabilities.
- On-Line Tests (OLTs) for I/O units are run under OLTEP for concurrent I/O maintenance.
- □ OLTs are run off-line under OLTSEP.
- ☐ System Test/370 which is self-configuring.
- Functional packaging of the processor logic,
- A group of channels can be configurd off-line and maintenance performed concurrent with the customer operating the rest of the system.
- □ A dual console, 1 operator's and 1 support, with reconfiguration capability if operators console fails.
- Remote Support Facility (RSF) with down line logout analysis.



Technology

The 3033 Processor Complex uses the following Monolithic System Technology:

- □ MST-1
- □ MST-2
- □ MST-4
- □ MST-255
- □ MST-A
- □ MS-195

The Reloadable Control Storage (RCS) and the high-speed buffer use Advanced Bi-Polar Monolithic technology.
The processor storage employs MOSFET. (Metal-Oxide Semiconductor Field Effect Transistor) technology.

Performance

The throughput performance of the 3033 Processor Complex is enhanced through the use of the System Configuration, the Operating System and the program job stream. The high perormance achieved is attributed to:

- The high speed and reliability of the technologies.
- □ A processor cycle of 60 nanoseconds.
- □ A 64K high speed buffer storage.
- □ Multiple instruction and operand buffers.
- Overlap of instruction and execute cycles.
- Eight way interleaved high performance processor storage.
- □ Translation lookaside buffer.

A System/370 Extended Facility, when used with MVS/System Extensions provides significant throughput enhancement for MVS.

Availability

The high availability of the 3033 Processor Complex is attained through automatic recovery techniques which permit deferred maintenance.

Instruction Retry will, for most instructions (except Execute, Diagnose, Read Direct (RDD) Write Direct (WRD), and Test and Set (TS), completely re-execute the instruction following an error condition provided the retry threshold is not exceeded.

Channel Recovery achieved through repetitive bardware retry and refresh of microcode instructions. Additional retry techniques are provided through software recovery supports.

Error Correcting Code (ECC) will correct single bit storage data failures without interruption of the system.

Multiple bit storage errors can be deferred through software recovery using page refresh or deletion.

The Recovery Management Support (RMS) supplements hardware executed automatic retry facilities. RMS assesses the software damage and repairs or selectively terminates the task.

Two megabyte increments of processor storage can be configured off-line, enabling the system operation to continue.

The Following Features will be available on all systems:

- System 370 Univeral Instruction Set
- System 370 Enhancement Instruction Set
- Byte Oriented Operands
- Direct Control
- Intervla Timer
- TOD Clock and Clock Cemparator
- CPU Timer
- Program Event Recorder (PER)
- 64K Byte High Speed Buffer
- Extended Control Mode
- Dynamic Address Translation (DAT)
- Storage Configuration Control
- Dual Purpose Console with Service Support Facility and CRT Display
- Two groups of 6 channels each
- Floating point
- Extended Precision Floating point
- External Signal
- Conditional Swapping
- PSW Key Handling
- 4 MB Storage
- System/370 Extended Facility

Optional Features

- Extended Channel Feature
 4 Additional Channels
- Channel to Channel Adapter
- Two Byte Channel Interface
- Six or Eight Megabytes of Storage.

Processor Complex (PC)

The PC consists of an instruction pre-processing function (IPPF), an execution (E)-function, a processor storage control function (PSCR), processor storage and channels.

The IPPF fetches intstructions and prepares them for execution by the E-function. The IPPF also determines priority and makes fetch requests for instructions and operands.

The E-function executes the instructions prepared by the IPPF function and is capable of processing an instruction every cycle.

The E-function is primarily controlled by microprogramming within the control storage.

The PSCF processes all requests to store data into or fetch data from processor storage. Logical storage addresses are converted into real storage addresses for addressing processor storage. The PSCF also provides for execution of the Invalidate Page Table Entry (IPTE) instruction.

The processor storage is an integrated monolithic non-destructive readout storage. The storage technology is the MOSFET type. The processor storage is available in capacities of 4, 6 and 8 megabytes. The storage operates in a serail or eight-way interleave mode and a double word data width. The processor storage control function contains the Dynamic Address Translation (DAT), Translation Lookaside Buffer (TLB), high speed buffer, address array, storage protect, and channel buffers.

The control storage consists of 8K bytes of Reloadable Control Storage (RCS) for each channel group, 6K bytes of Writable Control Storage (WCS) in the E-function, and 64K bytes of FET storage for each of the 2 console processors.

Channels

The 3033 Processor Complex has 12 integrated channels on the basic machine which can be extended to 16 integrated channels.

The basic channels are sub-divided into groups consisting of 1 byte and 5 block multiplexer channels and a common logical function. The extended group consists of 4 additional channels.

The 2 byte feature can be applied to the first block multiplexer in each group.

Each logical function is micro-program controlled and consists of 8K words of Reloadable Control (RCS), 8K words of Bump Storage, 64 words of data local storage and 48 words of UCW local storage.

CE Career Path

This is a "General Systems" product.

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DP Customer Engineering
EHQ - Paris, France
A/FE - New York, U.S.A.

Printed in Western Germany